Ka/Q BAND GaAs IMPATT AMPLIFIER TECHNOLOGY

G. Jerinic, J. Fines, M. Cobb, and M. Schindler

Raytheon Research Division
131 Spring Street
Lexington, MA 02173

Abstract

    GaAs IMPATT diodes are capable of generating 2 to 3 W simultaneously with 18-22% efficiency in the 33 GHz to 46 GHz frequency band. The design of the amplifier cir- cuits which utilize these devices is discussed. The circuit design is based on a 3-step closed form algorithm. The first step is a passive circuit characterization with an automatic network analyzer. In the second step, a computer is used to generate diode device lines. The third step is load line synthesis for predictable opera- tion. The resulting performance is described. 2 W over a 2GHz bandwidth was achieved simultaneously with a min- imum gain of 12 dB.

Introduction

In Ka (33–36 GHz) and Q (36–46 GHz) bands, the IMPATT diode is the only solid state device capable of high power generation. The properties of the two most commonly used device types are discussed.

The design of high-power IMPATT diode circuits is complex because these two-terminal devices present a negative resistance over a broad frequency range, and their impedance is very low. Therefore, they are difficult to match for high power generation and to control. One can obtain an occasional impressive result empirically; however, for predictable and repeatable operation, sound design procedures must be used. A procedure based on Sparameter circuit circuit characterization with an automatic network analyzer[1-4] is discussed, and examples of the state-of-the-art performance achieved with such circuits are given.

IMPATT Diode Considerations

At millimeter wavelengths, the IMPATT diode is the only solid state device capable of high output power generation. Two types of diodes are commonly used:

1. Gallium arsenide (GaAs) double-drift IMPATT diodes
2. Silicon (Si) double-drift IMPATT diodes

The performance achievable with these devices in Ka and Q band is:

Power (P_{rf})	2–3 W
Thermal resistance (θ_T)	18–22°C/W
dc-to-rf conversion efficiency (η)	10–12% (Si)
	18–22% (GaAs)

The diode junction temperature is the key factor which affects reliability of operation. The relationship between the mean time to failure (MTTF) and the junction temperature is shown in Fig. 1 for both Si and GaAs diodes. Typically, for reliable operation the junction temperature should be less than 250°C. This reliability consideration constrains both the maximum allowable ambient temperature and the maximum dc bias power. Junction temperature is a function of the ambient temperature, the thermal resistance
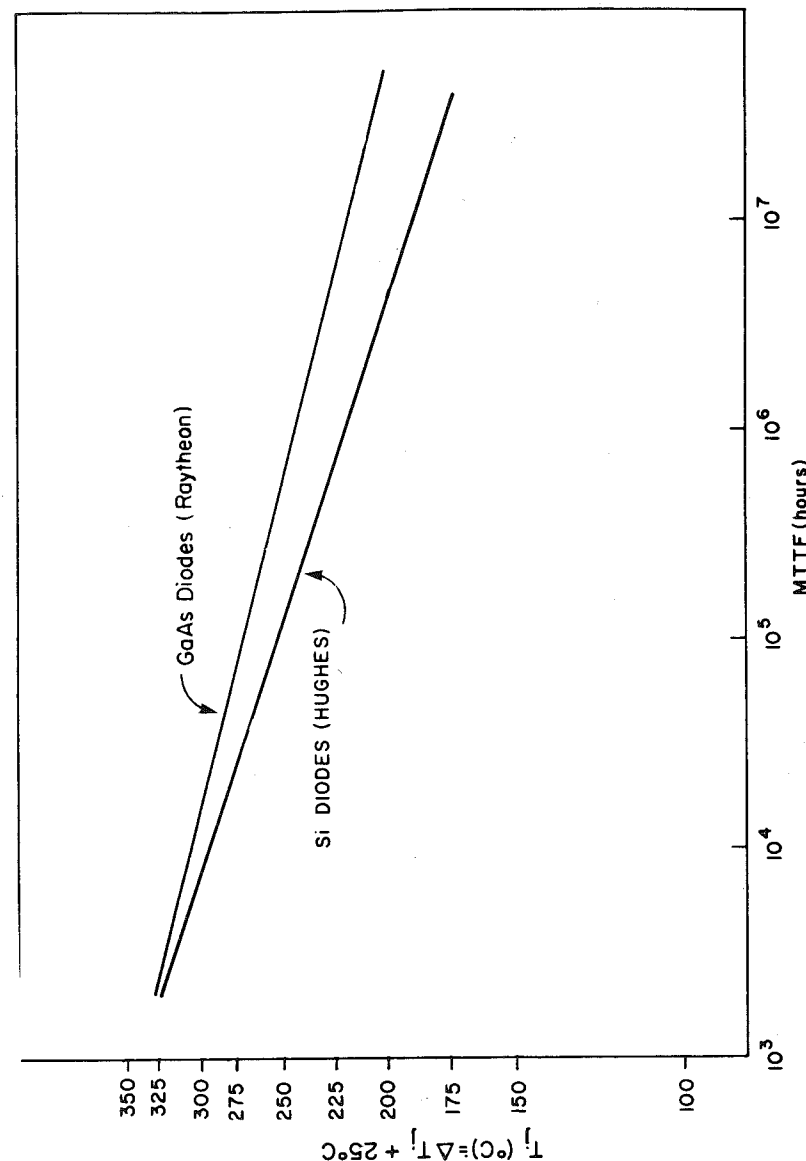
Figure 1. Reliability performance of GaAs and silicon diodes.

(from junction to ambient), and the bias power dissipated in the junction:

$$T_j = T_A + \Theta_T \cdot P_{diss}$$

$$T_j = T_A + \Theta_T (P_{dc} - P_{rf})$$

$$T_j = T_A + \Theta_T P_{rf} (1/\eta - 1)$$

$$\Delta T_j = T_j - T_A = \Theta_T P_{rf} (1/\eta - 1)$$

where

T_j	=	diode junction temperature in °C
T_A	=	ambient temperature in °C
Θ_T	=	thermal resistance in °C/W
P_{diss}	=	power dissipated in the junction in watts
P_{dc}	=	dc bias power in watts
P_{rf}	=	rf power generated by the diode in watts
η	=	dc-to-rf conversion efficiency.

Hence, efficiency and thermal resistance are the keys to reliable operation. Because of the inherently higher efficiency of GaAs IMPATT diodes, this technology has been pursued at Raytheon during the last 13 years, resulting in the state-of-the art devices shown in Fig. 2. The following results are pertinent to the present discussion:

1. 3 W simultaneously with 22% conversion efficiency was achieved at 35 GHz.

2. 2 W and 18% was obtained at 44 GHz.

In order to minimize the thermal resistance, diodes are mounted on diamond heatsinks. With this technique, 14-15°C/W is the best achievable Θ_T at these frequencies; however, a more typical range is 18-22°C/W.

Figure 3 summarizes the above discussion. It shows the relationship between ΔT_j and P_{rf} for the two extreme cases:

1. Worst case: η = 18%, Θ_T = 22°C/W
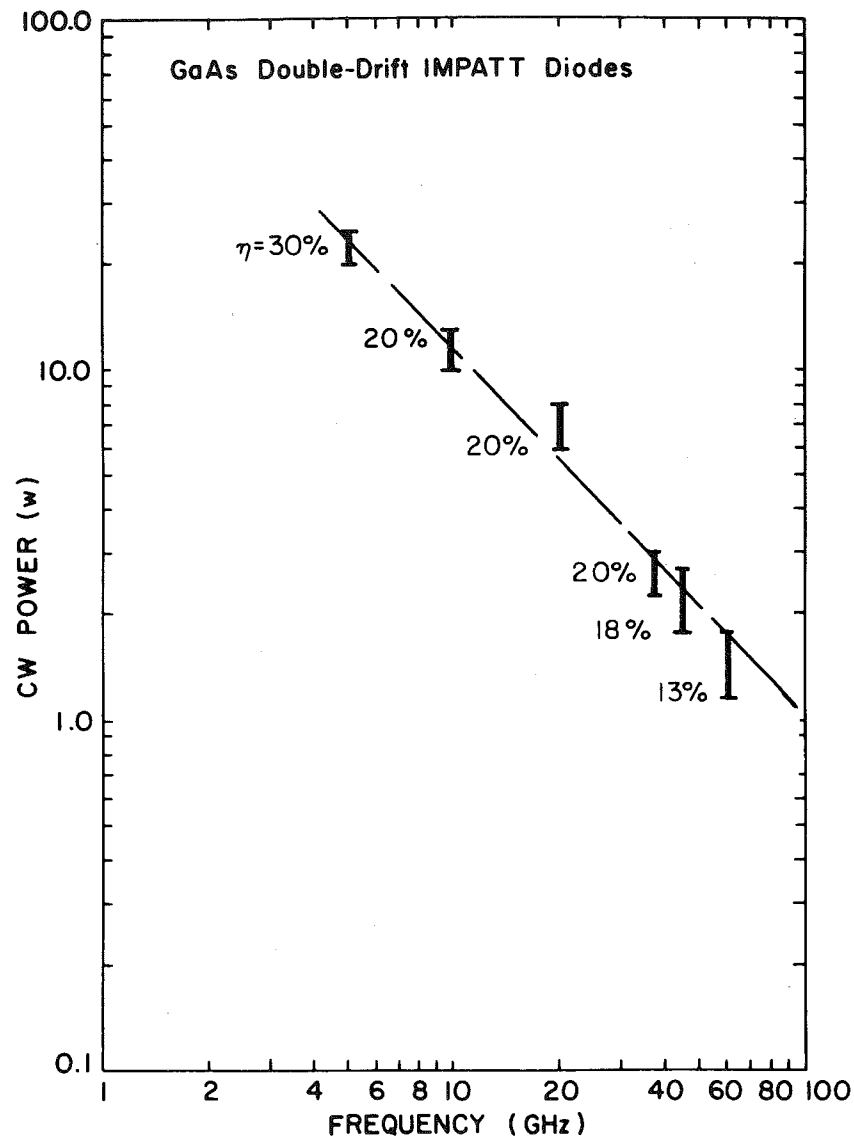2. Best case: η = 22%, Θ_T = 18°C/W

Figure 2. Performance of GaAs double-drift CW IMPATT diodes.
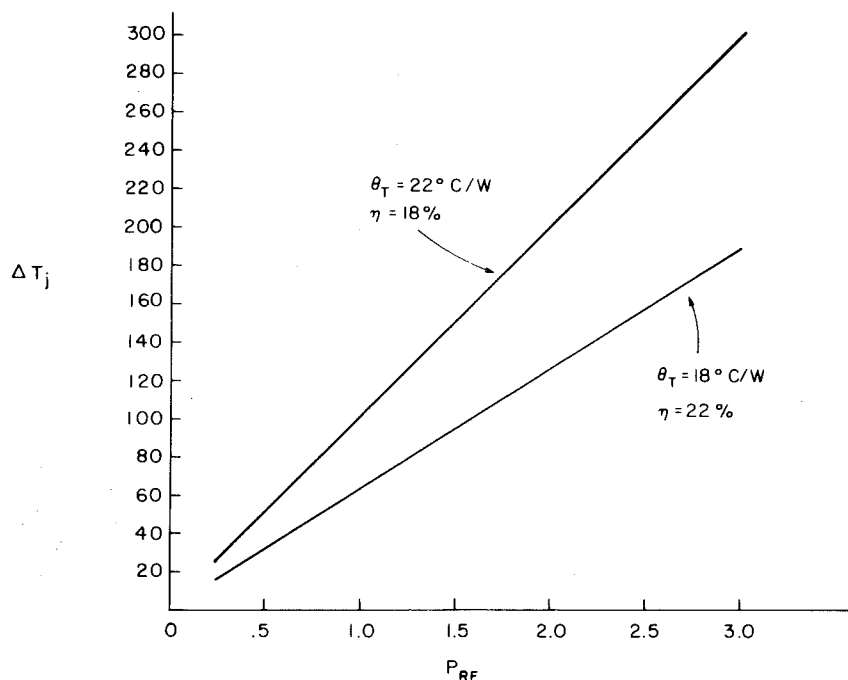
Figure 3.   Junction temperature rise above ambient
             ambient as a function of rf power.

For a minimum desired device MTTF, one can determine the
maximum allowable T_j from Fig. 1. ΔT_j is the difference
between this T_j and the maximum ambient temperature. From
ΔT_j and Fig. 3, the rf power obtainable from a single
diode can be determined.

For some applications the power obtainable from a
single diode is sufficient. However, in most cases, the
power from a number of devices must be combined. The
design and the performance achievable with single- and
multi-diode circuits is discussed next.

DESIGN PROCEDURES

The IMPATT diode is a two-terminal, negative-resist-
ance device which can operate as a free-running oscillator,
an injectionlocked oscillator, or a negative-resistance
amplifier. The mode in which the diode will operate
depends on diode characteristics, the impedance presented
to the diodes by the embedding circuit, and the amplitude
of the signal to be amplified. Hence, the design of an
IMPATT diode circuit can be divided into three parts:

1. IMPATT Diode Characterization. The impedance or
    admittance of the diode is determined as a func-
    tion of frequency and rf power level.

2. Selection of Mode of Operation. The impedance
    which must be presented to the diode by the
    circuit for a particular mode of operation and
    power level is determined.

3. Passive Microwave Circuit Design. A circuit
    which presents the appropriate impedance to the
    diode is designed.

These design steps are quite general. They are valid
for both Si and GaAs IMPATT diodes and for single- and
multi-diode circuits. They not only lead to circuits with
predictable and repeatable performance, but are also useful
for predicting the optimum performance that can be achiev-
ed.

Figures 4 and 5 will be used to illustrate these
three steps. Shown in Fig. 4 is a simplified schematic
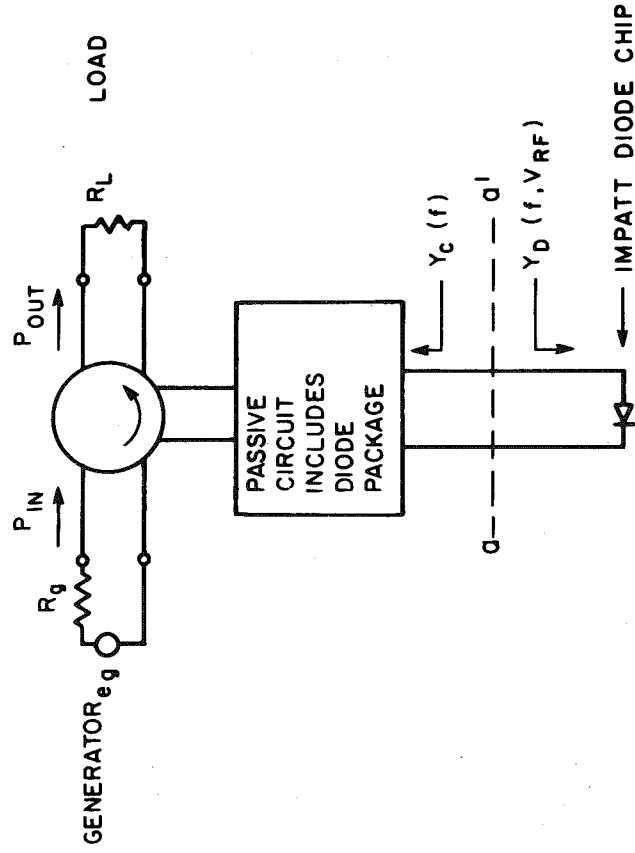diagram of a single diode amplifier circuit; Fig. 5 is an

Figure 4. Schematic diagram of injection-locked IMPATT diode oscillator or negative resistance amplifier.
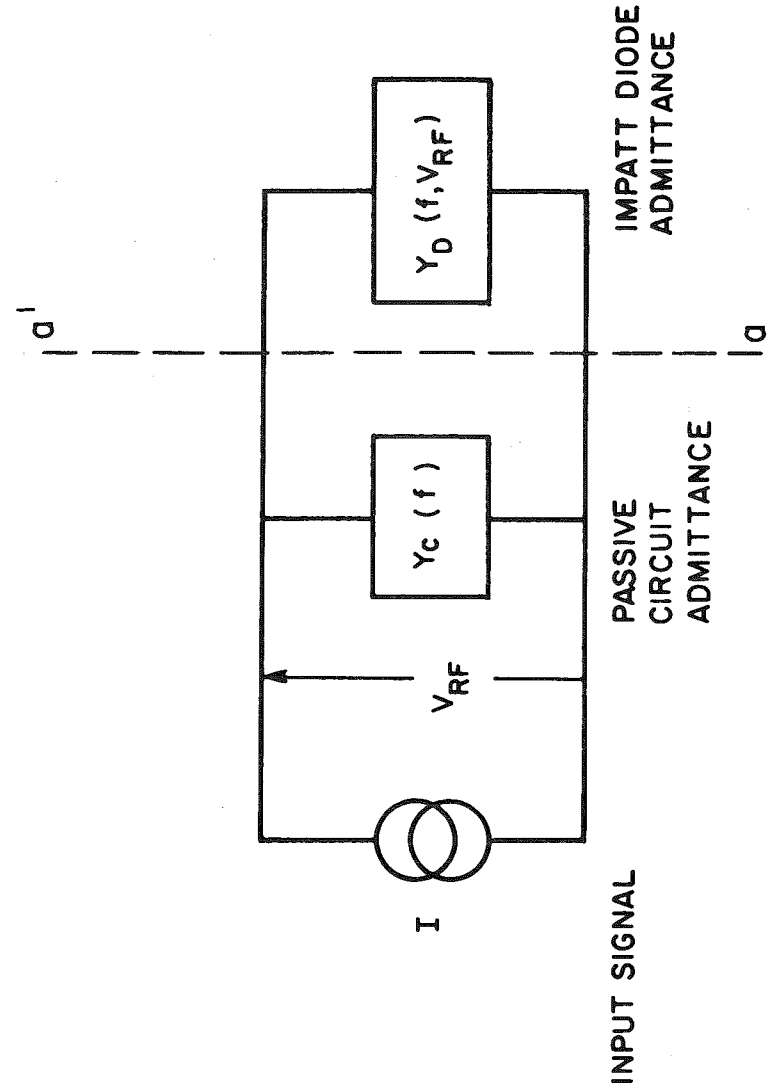

Figure 5. Simplified equivalent circuit of injection-locked IMPATT diode oscillator or negative resistance amplifier.

equivalent circuit (at reference plane aa') for such an amplifier. $Y_D(f,V_{rf})$ is the IMPATT diode admittance as a function of rf voltage and frequency.

$V_{rf}(f)$ is the rf voltage amplitude across the IMPATT diode chip terminals.

f is the operating frequency.

$Y_C(f)$ is the circuit admittance as a function of frequency.

I(f) is the rf current due to the signal which must be amplified.

The equivalent circuit in Fig. 5 is very general and can represent a free-running oscillator (by setting I=0), an injection-locked oscillator, or a negative resistance amplifier. In the case of a free-running oscillator, the circulator is not necessary but is frequently used as an isolator (the generator is replaced by a matched load in Fig. 4). In a single- or multidiode amplifier circuit, the circulator or a 3 dB hybrid coupler must be used to separate the input from the output. Two examples of such multidiode amplifying circuits are shown in Fig. 6. In all cases one can generate equivalent circuits (at reference planes aa') as shown in Fig. 5; hence, the three design steps are the same.

Impatt Diode Characterization

To design an IMPATT amplifier or oscillator, one must know the device impedance or admittance for a specific dc bias as a function of frequency and rf voltage. This data can be generated by computer modeling or directly measured in the laboratory. Computer modeling has the advantage of speed, but its validity must be confirmed by measurement for each circuit type, frequency, and rf voltage range. Figure 7 is a schematic representation of the automatic (computer-controlled) network analyzer used for device characterization in Raytheon's Research Division Laboratory. The analyzer and accompanying software are not available commercially. The impedance of an IMPATT diode at the design frequency depends on the impedances presented to the diode at harmonic and subharmonic frequencies.
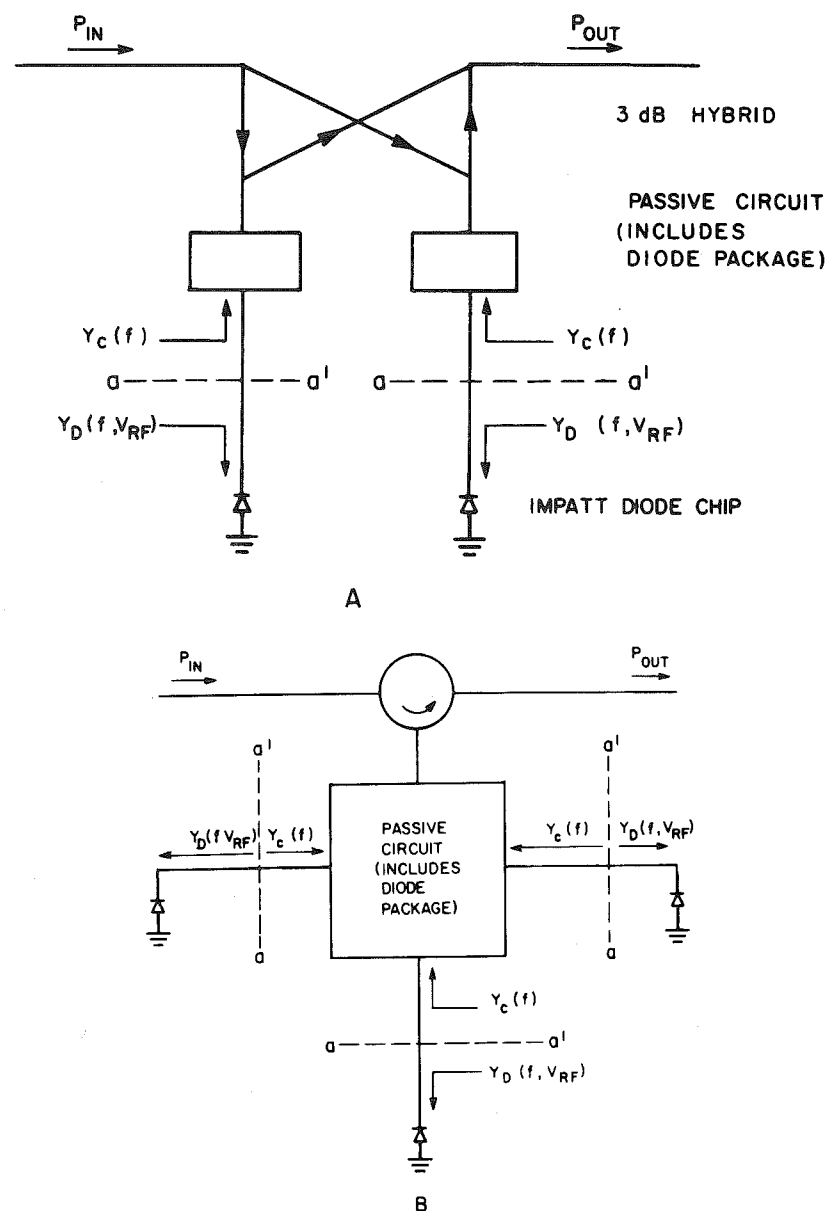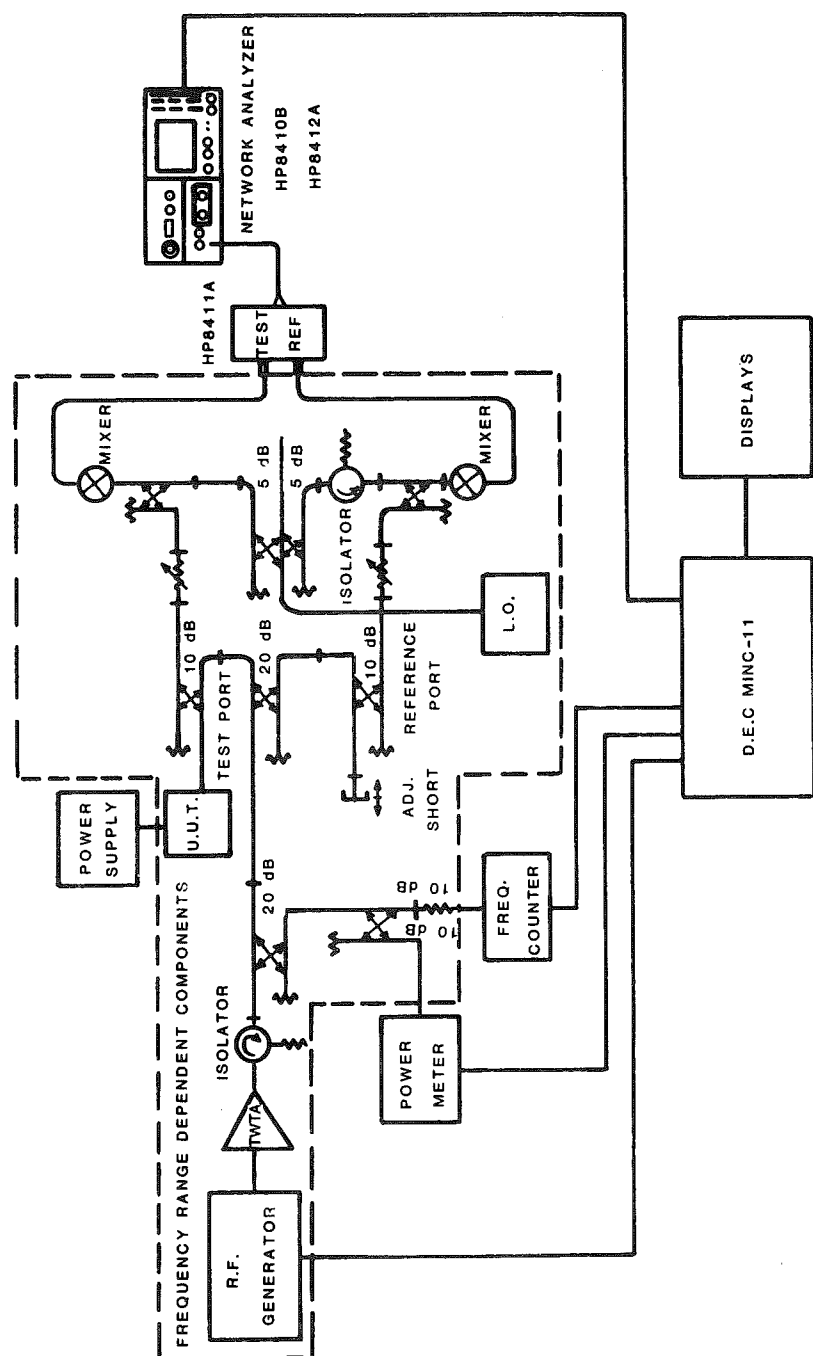
Figure 6.   Examples of multi-diode circuits.

Figure 7. EHF computerized large signal network analyser.

Hence, a diode impedance measurement depends on the circuit in which the diode is embedded.

Admittance plots for typical Raytheon GaAs double-drift diodes (optimized for 35 GHz and for 44 GHz) are shown in Fig. 8. This data was generated by computer. In the model used, it was assumed that harmonic and subharmonic frequencies were shorted.

Direct measurement is obviously more accurate than computer modeling but it is also much more time-consuming. For each new circuit and frequency range, the diode impedance plot generated by the computer model is confirmed by direct measurements at selected points. After confirmation, the computer model is used in the amplifier/oscillator design. The data shown in Fig. 8 has been confirmed by direct measurement with the analyzer shown in Fig. 7.

Selection of Mode of Operation

It can easily be shown (see Fig. 5) that the relationship between Y_D, Y_C, V_{rf} and I is:

$$Y_D + Y_C = I/V_{rf}$$

Since Y_D, Y_C and I/V_{rf} are related, it is obvious that only two of these quantities can be chosen independently. In most cases, the circuit designer begins with an existing IMPATT diode, so $Y_D(f,V_{rf})$ is given, leaving $Y_C(f)$ or I/V_{rf} under his control.

The rf power that the diode can generater at any frequency can be calculated from $Y_D(f,V_{rf})$ using the expression

$$P_{rf} = 1/2 \ V_{rf}^2 \cdot R_e \left(-Y_D(f,V_{rf}) \right)$$

For example, if the 44 GHz diode described by Fig. 8b is embedded in a circuit adjusted so that $V_{rf} = 12$ V, it will generate 2.3 W. If $Y_C(f)$ is changed (the circuit is retuned) so that V_{rf} is 12 V at 35 GHz, the diode will generate 2.2 W. Similarly, the same device can generate 1.9 W at 50 GHz. It is not possible to design a single circuit which can fully utilize this broadband power generating capability. By analyzing the relationship between I/V_{rf},
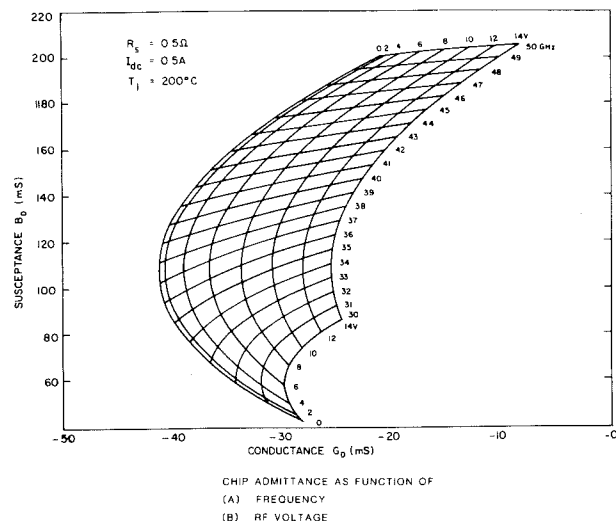
Figure 8a.   GaAs IMPATT diode chip admittance as a function of
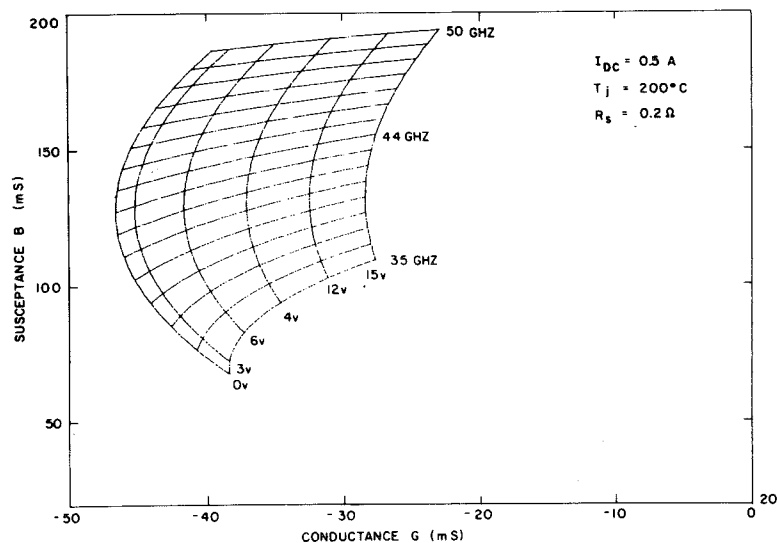   frequency and rf voltage for a 44 GHz device.

Figure 8b.   GaAs IMPATT diode chip admittance as a function of
             frequency rf voltage for 35 GHz device.

Y_C and Y_D, one can determine the dependence of power and
bandwidth on I/V_{rf} or Y_C for the particular Y_D. Kurokawa[5]
has developed an elegant graphical analysis which gives
insight into performing the trade-offs between power,
bandwidth, gain and stability.

In this analysis, one plots Y_D, the negative of Y_C,
and I/V_{rf} on the same complex admittance plane; from the
relationship of the admittance contours and the I/V_{rf}
vector one can determine the proper Y_C and input power.
For example, for the free-running oscillator case (where
$I=0$), the condition for oscillation is:

$$Y_D(f,V_{rf}) = -Y_C(f)$$

A graphical solution of this expression is obtained at the
intersection of the two admittance contours: Y_D and $-Y_C$,
as shown in Fig. 9. Y_D is usually referred to as the
device lines; $-Y_C$, as the load line. The above relation-
ship describes idealized oscillations at the desired fre-
quency, f_o, and ignores such complications as bias circuit
oscillations, instabilities, parametric oscillations and
harmonic termination effects.

For a given frequency, there is a small range of rf
voltage amplitudes over which a diode will operate with
maximum poweradded efficiency. This determines the desired
diode operating point and the circuit admittance required
to achieve high-power, high-efficiency operation. In Fig.
9, the common frequency at which the load line and the
device lines intersect is f_o. As the load line is varied
(by tuning the circuit), the operating point can be moved
along the f_o device line until the point of peak output
power is located. In Fig. 9, the dashed line indicates
this maximum power point. Note also that as frequency
increases from f^- to f^+, the load line and device line
admittances "move" in opposite directions; hence, there is
only one frequency at which they intersect (f_o). The load
line shown in Fig. 9 is characteristic of a single-tuned
circuit. In a doubletuned circuit, the load line loops,
so that there may be several common frequencies at which
the load line and the device lines intersect. These
multiple intersections will result in oscillator frequency
jumping and erratic, unstable free-running oscillator oper-
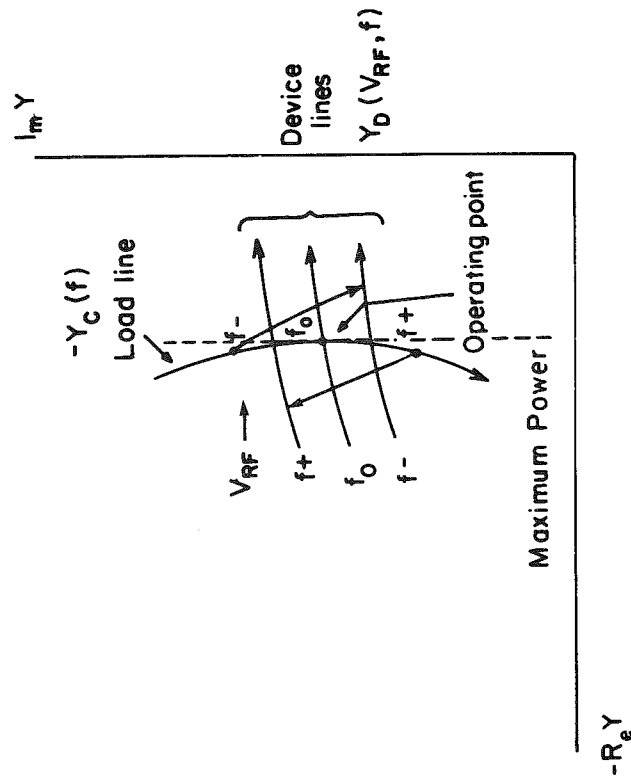ation.

Figure 9. Complex admittance plane illustrating a set of device lines, the load line and the operating point at frequency f_o.

The intersection of device and load lines is a necessary but not sufficient condition for satisfactory free-running oscillation. The angle of intersection is also important. The device lines can be thought of as vibrating in both the longitudinal and transverse directions, which results in both AM and FM noise. For a perpendicular device line, load-line intersection noise will be at a minimum. For small intersecting angles, noise will increase and bias circuit instabilities may also result.

If an input signal of frequency f^- is present, an oscillator with a free-running frequency f_o can be made to oscillate at f^-. This situation is also shown in Fig.9. The locking vector "bridges" the gap between the load line admittance at f^- and the device line f^-. The length of the vector is equal to I/V_{rf} and is proportional to the power in the locking signal. (The same discussion holds for f^+, which is also shown in Fig. 9) If the locking signal frequency is f_o, the power will decrease as the locking signal amplitude increases. This is true because the load line and the device line intersect at the maximum power point and the injected signal will move the operating point away from this optimum condition toward smaller negative conductance ($-R_e Y$). Hence, for locked operation, the load line and device lines should intersect to the "left" of the maximum power point, as shown in Fig. 10. The greater the separation between these two points, the longer the locking vector must be to "bridge" them. The longer the vector, the more powerful the locking signal must be, and since the maximum diode power is constant, the lower the locking gain.

For amplifier operation the load line position should be such that there are no common frequency intersections with the device lines. For this case the diode will not generate rf power unless there is an input signal. Such a circuit is called an (absolutely) stable amplifier. Unfortunately, stable operation usually requires a considerable reduction in the amplifier's output power from the diode's maximum available power if fixed gain is required. Alternatively, the amplifier can operate with maximum available output power, but with a significant reduction in gain.
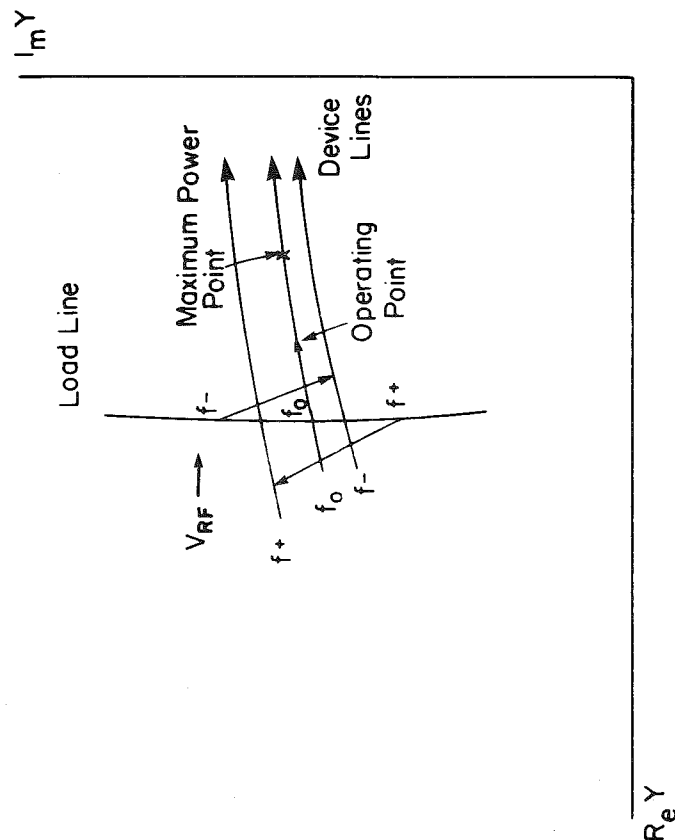
Figure 10. Admittance plane for locked operation.

To avoid these difficulties, an amplifier can be operated in the conditionally stable mode. In this type of operation, the load line intersects the device lines in the low V_{rf} region. The amplifier will oscillate, somewhat noisily, at a reduced power level (usually about -6 dB from the maximum output) in the absence of an rf drive. The advantage of this mode of operation is the ability to reach maximum available power output while maintaining reasonable gain levels.

If the frequency varies slowly along the load line, large changes in frequency will cause only small changes in the load line to operating point separation and the amplifier will have a large gain bandwidth product.

The optimum relationship (for stable amplifier operation) between device lines and the load line is shown in Fig. 11. The load line does not intersect the device lines at any frequency, so the amplifier is absolutely stable. The distance from the load line to the region of high diode efficiency is sufficiently large that gain compression will be minimized, but sufficiently small that that the amplifier retains moderate gains at high power-added efficiency. Finally, the frequency changes slowly along the load line so bandwidth will be broad.

In summary, when a circuit has been designed to include the presence of an input signal, three possibilities exist for the output power when the input signal is removed:

1. The power level can change slightly.
2. The power level can change substantially.
3. The power level can drop to zero.

In all three cases, the frequency of operation will change. The behavior described by the first case is indicative of the injection-locked oscillator mode of operation. If the behavior is as described by the third case, the circuit is a stable nega tive resistance amplifier. The second case can be labeled either a locked oscillator or a conditionally stable amplifier. Its key characteristic is an oscillation in the absence of an input rf signal. If the level of oscillations is very low (~ -6 dB), this mode of operation is usually labeled a conditionally stable amplifier. As the level increases,
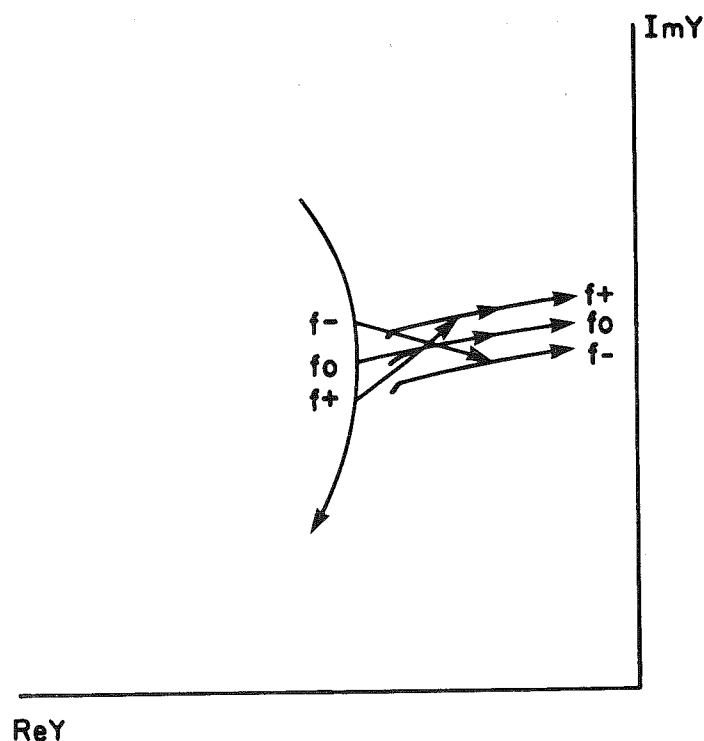
Figure 11.   Optimum relationship between device and load line.

it becomes a question of personal preference when to switch the label from amplifier to injection-locked oscillator.

To obtain broad bandwidth requires minimization of the variation of Y_C with frequency. Gain flatness implies controlling the separation between $Y_D(f,V_{rf})$ and $-Y_C(f)$. The actual gain value can be calculated from the well-known expression[6]

$$G = \left| \frac{Y_D^*(f,V_{rf}) - Y_C(f)}{Y_D(f,V_{rf}) + Y_C(f)} \right|^2$$

The power generated by the diode, the gain, the frequency of operation, the bandwidth and the mode of operation (or stability) are interrelated and controllable by the circuit in which the diode is embedded. Typical relationships between these parameters, which can be realized practically, are summarized in Table 1 for each mode of operation.

Passive Microwave Circuit Design

As the previous discussion showed, the gain, the power added by the diode, the mode of operation and the bandwidth are interrelated and dependent on the relative positions of the load line and the device lines in the complex admittance (or impedance) plane. We now discuss a process for generating an appropriate load line. Obviously, the circuit choice plays a key role in determining which load lines are physically realizable. Two of the most suitable single diode structures are shown in Fig.12 and two multidiode structures are shown in Fig 13. All of these circuits have a single port and hence require a circulator to separate input from output.

The single-diode, "top-hat" circuit, shown in Fig. 12a is widely used for diode testing. The impedance presented to the diode is controlled by the diameter of a disk ("top-hat"), the movable-waveguide short circuit, and the position of the coaxial choke (which prevents the dc bias circuit from interacting with the rf circuitry). This circuit is capable of presenting an extremely wide range of impedance (admittance) values to the diode, which is obviously an advantage in a test circuit. Its

TABLE 1
CHARACTERISTICS OF VARIOUS MODES OF OPERATIONS
(HIGH-POWER, LARGE-SIGNAL CASE)

TYPE OF OPERATION	Gain	Characteristics	Bandwidth
Free-running oscillator	∞	Full power output at operating frequency	Single frequency
Injection-locked oscillator	8-20 dB	High power output near operating frequency	< 5%
Conditionally stable negative resistance amplifier	5-8 dB	Low power output may be far from operating frequency	5% to 10%
Stable negative resistance-amplifier	< 5 dB	No rf output	> 10%

For all cases:
    Output power   - High
    Power-Added Efficiency - High
    AM-to-PM Conversion   - Moderate
    FM Noise   - Requires low-noise drivers
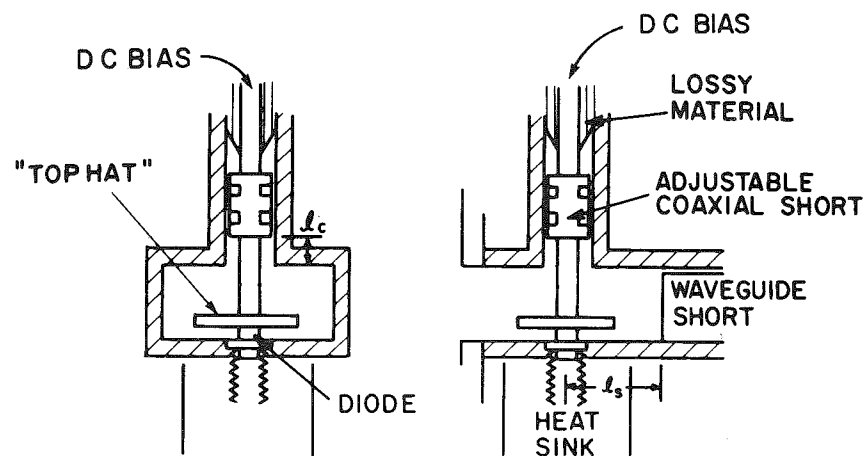
A) "TOP HAT" CIRCUIT.
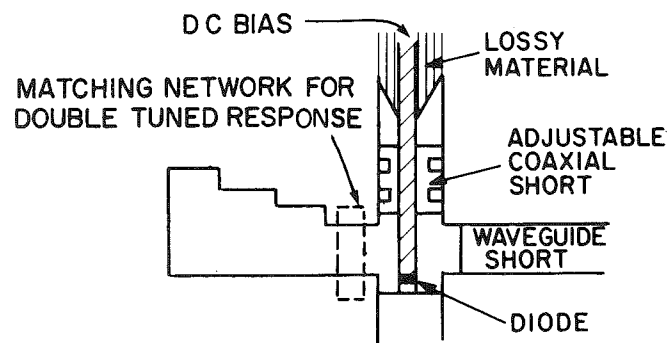
B) REDUCED-HEIGHT WAVEGUIDE CIRCUIT.

Figure 12. Single-diode amplifier design approaches.

main disadvantage is that this impedance is a very sensi-
tive function of the above three parameters, so that such
a circuit is difficult to reproduce.

    The circuit shown in Fig. 12b is the most widely
used in broad-bandwidth applications. The diode is mount-
ed in a coaxial line which is coupled to a reduced-height
waveguide. The reducedheight waveguide is matched to a
full-height waveguide via multiple quarterwave transform-
ers. This is a very low Q structure and consequently the
impedance (admittance) presented to the diode varies slow-
ly with frequency. The position of the load line is
controlled by the positions of waveguide and coaxial
short circuits. The impedance can be even further local-
ized with the addition of a matching network, as shown in
Fig. 12b. This broadband matching network is used to
create "loops" in the load line, resulting in double,
triple, etc., tuned amplifier response. This same approach
can be used in broadbanding multidiode circuits.[4]

    To ensure that the outputs of many low-power ampli-
fiers (or oscillators) are efficiently combined, one must
suppress power-robbing modes. These modes always exist
when amplifiers (or oscillators) are coupled. In order to
suppress them, one must decouple the amplifiers (or oscil-
lators) while still assuring frequency coherence. Since
the IMPATT diode's negative resistance is extremely broad-
band, this decoupling must be accomplished not only at the
frequency of interest, but also at subharmonic and harmonic
frequencies.

    Both of the structures shown in Fig. 13 provide the
needed isolation between devices simultaneously with high
combining efficiency by employing a resonant cavity. In the
resonant cavity approach, each diode is mounted in a co-
axial line amplifier (or oscillator) structure which is
then magnetically coupled to a cavity resonator. The
cavity is the frequency-determining element, and it also
provides the physical space where rf power is combined
and delivered to the useful load. The coaxial lines are
terminated with resistors which absorb spurious frequen-
cies, resulting in stable IMPATT diode operation.

    The two most commonly used cavity types are cylindri-
cal and rectangular waveguide. The cylindrical cavity
resonates in TM_{0n0} modes. The coaxial modules are located
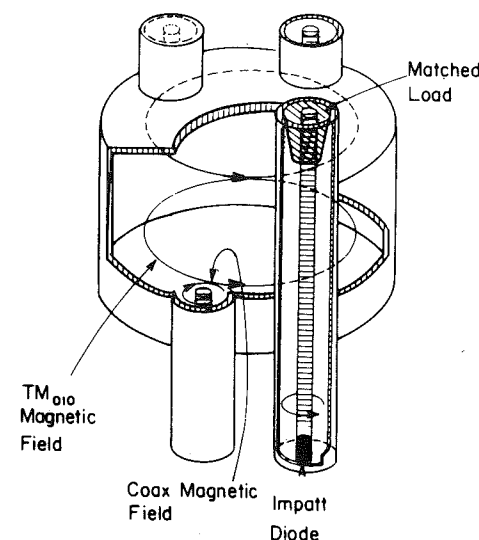
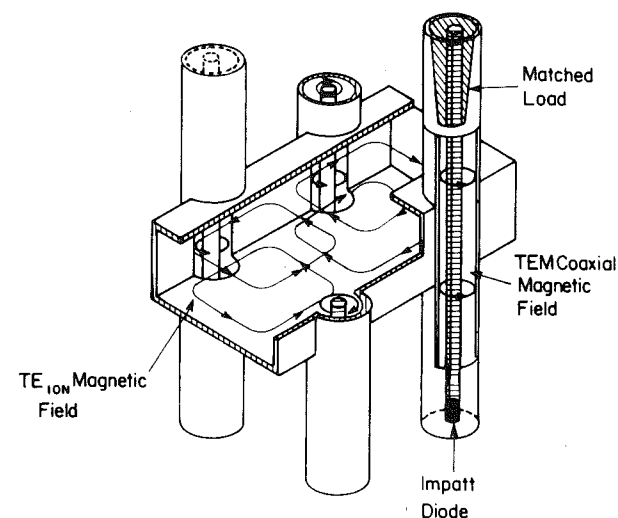CYLINDRICAL WAVEGUIDE CAVITY COMBINER

Figure 13.   Cavity combiner types.

at the circumference of the cavity, as shown in Fig. 13a.
The number of coaxial modules that can be fitted at the
circumference determines combiner diode capacity and, con-
sequently, the output power. Since cavity circumference
increases with n (TM_{0n0}), the combiner capacity also in-
creases. The rectangular cavity combiner resonates in
TE_{10n} modes. The coaxial modules are spaced at half-wave-
length intervals along the waveguide as shown in Fig. 13b.
To increase the combiner capacity, one must increase the
cavity length in half-wavelength steps. Since n is equal
to the number of half wavelengths, n also increases.
Hence, the two-diode rectangular cavity combiner resonates
in the TE_{101} mode, while the four-diode combiner is TE_{102}
and the six-diode is TE_{103}. At X-band, TM_{0n0} combiners are
most often used, because they are physically smaller than
TE_{10n} combiners of equal diode capacity. However, at
millimeterwave frequencies, the dimensions of the TE_{10n}
cavities are more suitable for fabrication (the size of
parts, spacing of diodes, etc.).

Lumped element models for the above structures are
frequently used to analyze their performance. The lumped
element values may either be computed from basic prin-
ciples or determined by measurement.

The equivalent circuit for a single-diode structure
(Fig. 12b) is shown in Fig. 14. All of the elements can
be calculated from the dimensions of the structure.[7]
This approach gives a good qualitative understanding of
the effects that various design parameters have on the
admittance presented to the diode.

Examples of multidiode equivalent circuits are shown
in Figs. 15 and 16. The individual lumped element values
are determined by measurements on a combiner with only
one diode line and are pieced together in a computer
circuit analysis program to evaluate the performance of
the complete circuit, which may contain many diodes.
Before discussing the type of information that can be
obtained from such circuit models, let us first briefly
discuss the principles of operation of the combiner struc-
ture.

Figure 15 illustrates the physical principles and
shows a simplified equivalent circuit for a resonant
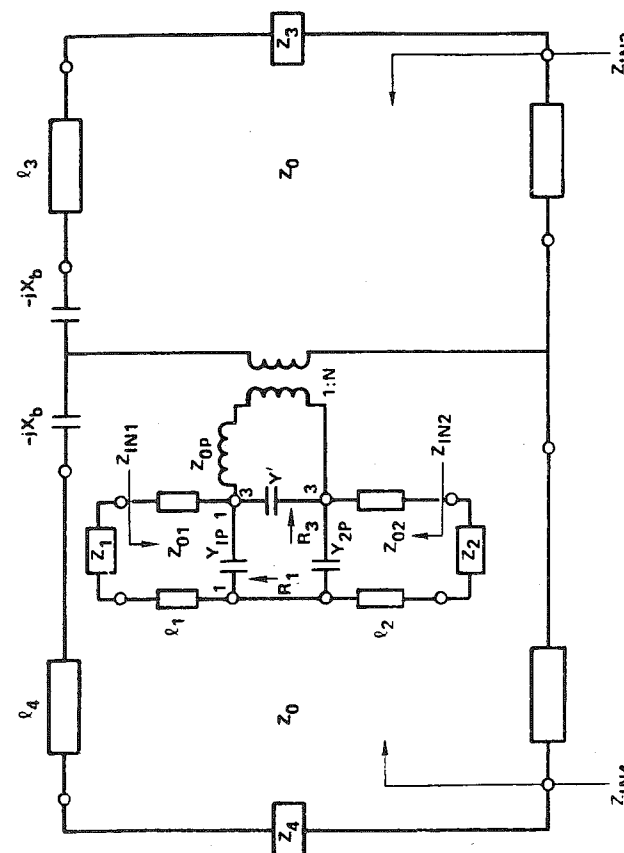cavity combiner. This figure shows the two-diode case for

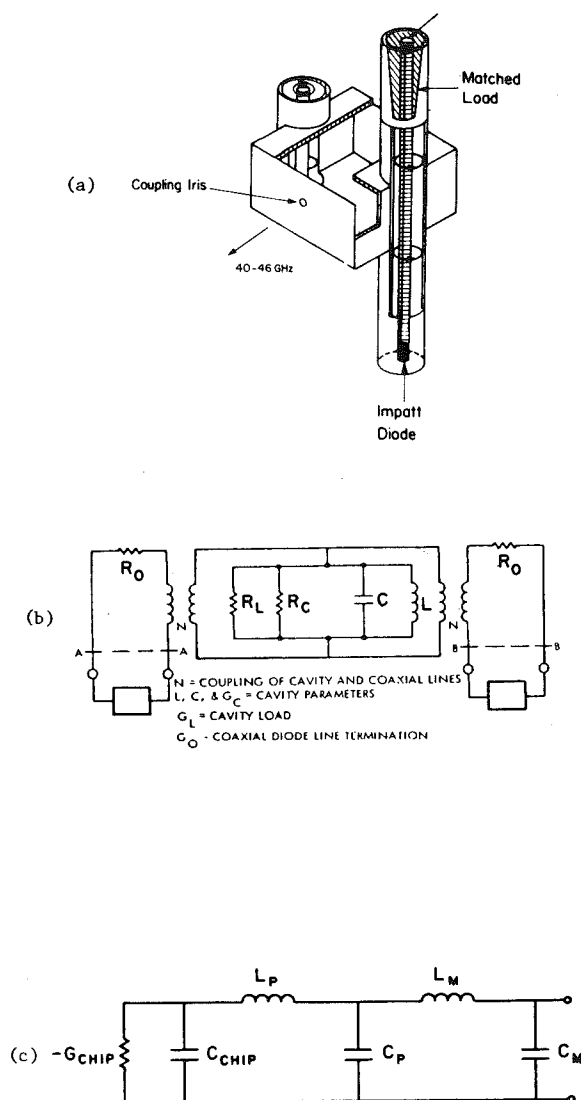Figure 14. Equivalent circuit for coaxially coupled waveguide mounting structure.[7]

(a)

Matched
Load

Coupling Iris

40-46 GHz

Impatt
Diode

(b)

N = COUPLING OF CAVITY AND COAXIAL LINES
L, C, & G_C = CAVITY PARAMETERS
G_L = CAVITY LOAD
G_O - COAXIAL DIODE LINE TERMINATION

(c)

Figure 15.   Resonant cavity approach, equivalent circuits
and physical principles: a) rectangular wave-
guide cavity combiner; b) equivalent circuit
near cavity resonant frequency; c) diode/
package equivalent circuit.

Where

Z_O = Characteristic impedance of the diode line

Z_O' = Characteristic impedance of the diode line as it passes through the cavity

Z_1 = Diode line load termination

$R_C, C_C, L_C,$ = Cavity parameters

N_d = Transformer coupling of diode to cavity

N_L = Transformer coupling of cavity to load

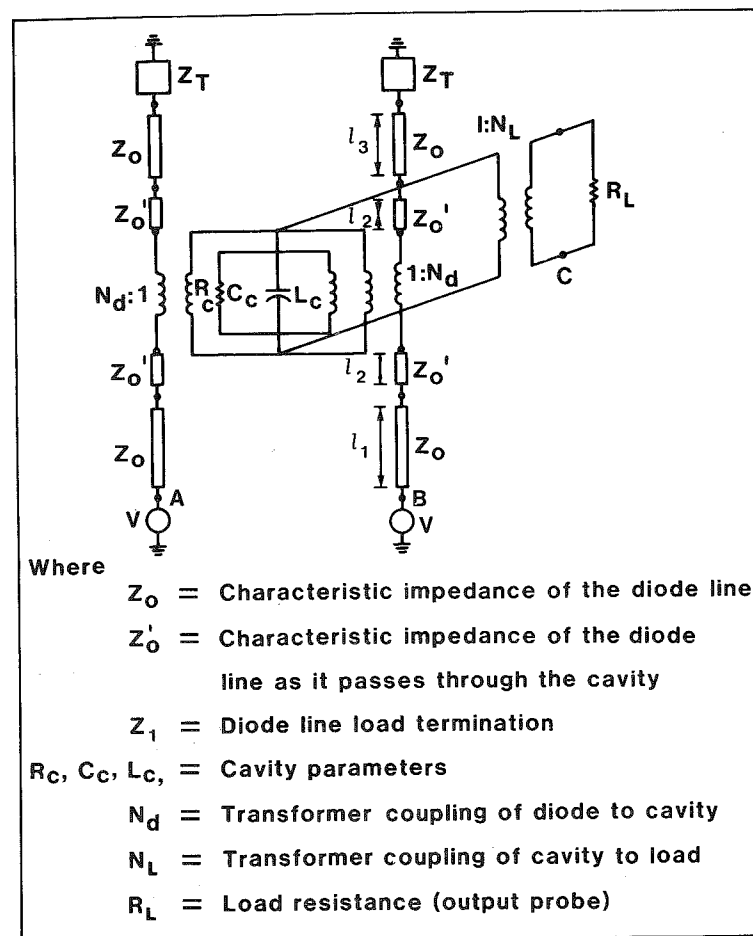R_L = Load resistance (output probe)

Figure 16.   Equivalent circuit for two-diode-line cavity combiner.

clarity, but extension to the multidiode is obvious. The
objective of the circuit represented in Fig. 15b is to com-
bine the rf power incident on ports AA and BB into the load,
R_L, at the design frequency. At all other frequencies, the
incident power should be dissipated in the loads R_0. To
accomplish this, the cavity impedance, "seen" at the input
ports AA and BB, must be real at the design frequency and
much larger than R_0. At all other frequencies, the cavity
impedance is small, so R_0 is the dominant factor.

The next design requirement is to ensure that the
IMPATT diodes generate their maximum power for combining
in the circuit. This is accomplished with a matching
network which transforms the impedances at planes AA and
BB in such a way that each IMPATT diode operates at the
design frequency, either as an amplifier at the desired
gain and output power or as an oscillator at maximum
power. Hence, the electrical design is conveniently div-
ided into three parts: design of the combining circuit
(passive microwave circuit design), single-diode charac-
terization, and design of the network which matches the
two (selection of mode of operation).

The design parameters that can be controlled and
optimized are:

$$N = \text{coupling of cavity and coaxial lines}$$
$$L_c,\ C_c \text{ and } R_c = \text{cavity parameters}$$
$$R_L = \text{cavity load (output coupling)}$$
$$R_0 = \text{coaxial diode line termination.}$$

The qualitative dependence of the combiner impedance,
loss and bandwidth on the above parameters and on fre-
quency can be obtained from an equivalent circuit, like
the one shown in Fig. 16.

Generally, an increase in the number of diode lines
increases the impedance presented by the cavity to the
diode lines. It also tends to decrease the circuit loss
(see Fig. 17). These trends may be shown using the equa-
tion for diode line impedance for a simplified version of
the circuit shown in Fig. 16. (The characteristic imped-
ance of the diode lines is assumed to be the same internal
to the cavity as it is external to the cavity, i.e., Z_0'
$= Z_0 = 1$.) The equation for diode line impedance (assuming
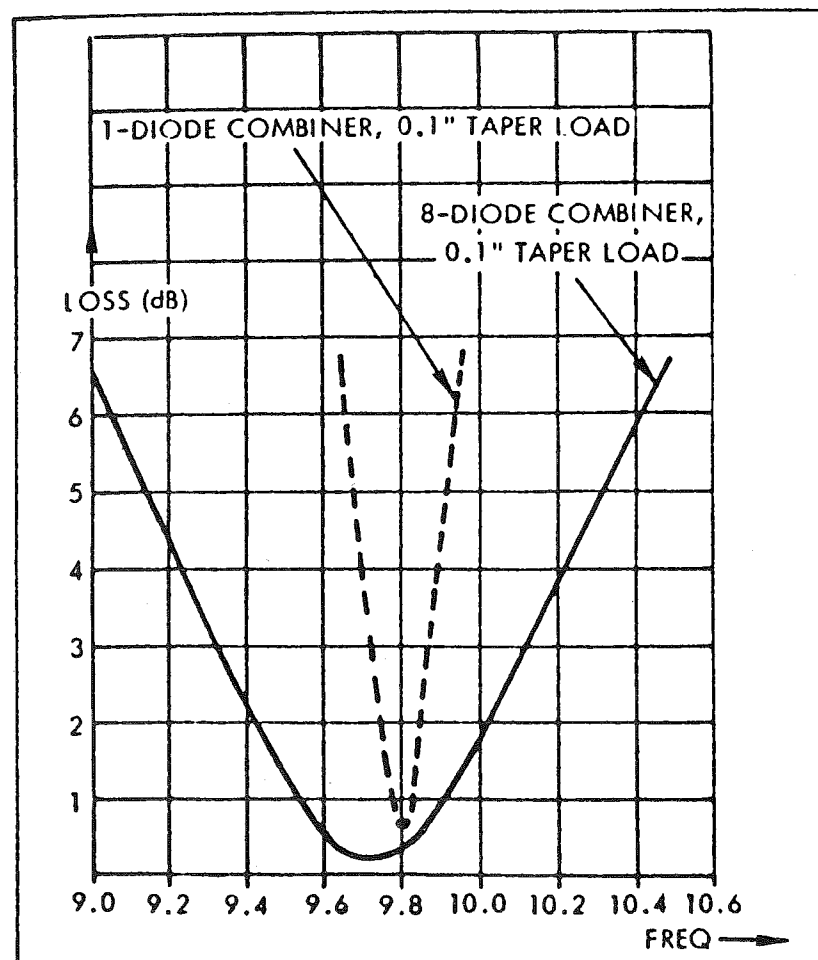all diodes are equiamplitude and equiphase) is given by:

Figure 17. Combiner loss vs. frequency computed
from lumped element model.

$$Z_d = Z_T + \frac{nN_D^2}{\left(\frac{1}{R_C} + \frac{N_L^2}{R_L}\right) + j\left(\omega C_c - \frac{1}{\omega L_c}\right)} \equiv Z_T + Z_{CAV}$$

$$= Z_T + R_{CAV} + j\, X_{CAV} \quad .$$

From this equation, it is obvious that the impedance increases when n, the number of diode lines, increases. Because the impedance presented by the cavity is in series with the resistance Z_T due to the resistive termination, an increase in n reduces the power lost in the termination and increases the power that can be delivered to the useful load.

Although lumped-element analysis has given good agreement with passive impedance measurements on circuits with a small number of diodes and is useful in obtaining a qualitative understanding of circuit behavior (necessary for circuit optimization), the extension of this method to circuits with large numbers of diodes and to the millimeter wave region has proven to have limited accuracy. A more accurate method has been developed and is presently employed for combiner characterization and optimization. This method utilizes a scattering matrix representation (Fig. 18).

An automatic network analyzer (see Fig. 7) is used to characterize the circuit alone (without diode(s)). The diode(s) are replaced with short circuit(s) and the reflection coefficient from the circuit output port is measured. By repeating this measurement for at least three short positions, the complete S matrix is obtained.[2] From the S matrix, the circuit efficiency and the impedance presented to the diode port (s) are determined.

The importance of circuit admittance in controlling diode performance has already been discussed, and now the circuit efficiency is defined. It is the ratio of the net power emitted at the output port (and absorbed the the external load) to the total power which enters the ports to which the diodes are attached. This definition results in a simple expression which is meaningful in this circuit design approach:
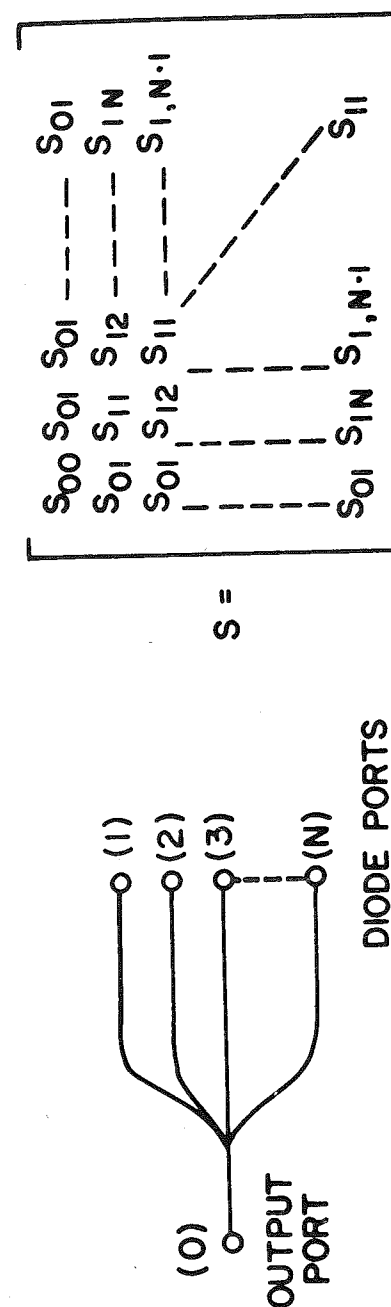
Figure 18. Scattering matrix for general combiner circuit.

$$E_{eff} = \frac{N|S_{01}|^2}{1 - |\sum_{n=1}^{N} S_{1n}|^2}$$

where

E_{eff} = circuit efficiency

N = number of identical input ports.

The S parameters are as defined in Fig. 18. This efficiency definition is an extension of the familiar operating power gain definition for a two-port network. This can easily be seen upon examination of the two-port network shown in Fig. 19. For a single diode ($N=1$) free-running oscillator case ($a_0 = 0$) which corresponds to the matched case $\Gamma_L = 0$, E_{eff} and G are identical:

$$E_{eff} = G = \frac{|S_{01}|^2}{1 - |S_{11}|^2}$$

For the injection-locked oscillator case, both a_0 and b_0 waves exist, $\Gamma_L \neq 0$, and the gain (and efficiency) expressions become more complicated. It can be shown that for the optimization of cavity-type multidiode circuits (Fig. 13) it is not necessary to use the more complex expression. Circuits optimized for the E_{eff} parameter will also be optimized when operated as injection-locked oscillators or negative resistance amplifiers.

By employing this circuit characterization technique, one can determine exactly what performance is obtainable (how lossy the circuit is, and from the admittance variation with frequency, what bandwidth and gain can be achieved). One also gains insight into what changes should be made in order to improve performance. One can characterize the circuit and modify it repeatedly until both the circuit admittance and efficiency are as needed to meet specifications. The key advantage is the fact that this optimization is performed on a passive circuit only. If the circuit being optimized contained IMPATT diodes, the optimization process would be extremely complex and the performance obtained would be a function of the time spent in the laboratory and of luck.
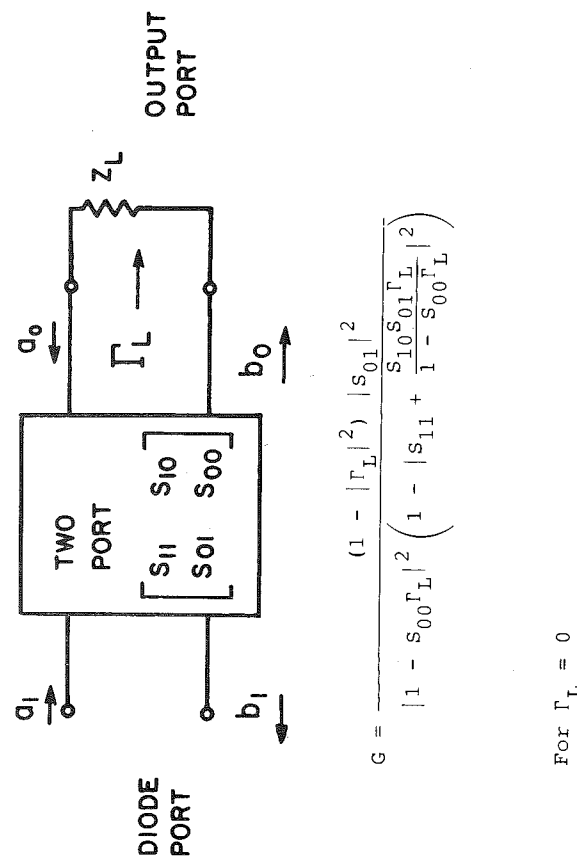

$$G = \frac{(1 - |\Gamma_L|^2)\,|S_{01}|^2}{|1 - S_{00}\Gamma_L|^2 \left(1 - |S_{11} + \frac{S_{10}S_{01}\Gamma_L}{1 - S_{00}\Gamma_L}|^2\right)}$$

For $\Gamma_L = 0$

$$G = \frac{|S_{01}|^2}{1 - |S_{11}|^2}$$

Figure 19. Operating power gain of a two-port network.

Performance

Using the S-parameter circuit characterization technique just described, the "top-hat" circuit was adjusted to present the load line shown in Fig. 20. With a 1.3 W diode, a state-of-theart bandwidth was achieved. Unconditionally stable amplification was obtained from 33 to 36.5 GHz. The output power varied from 0.6 to 1 W (Fig.21).

The exceptional bandwidth of this amplifier was achieved in two ways:

1. By assuring that the frequency varies slowly along the line load;

2. By controlling the shape of the load line:loop characteristic for a doubly resonant circuit.

A reduced-waveguide-height, single-diode circuit, shown in Fig. 12b was designed in a similar way, and it too achieved state-ofthe-art performance (Fig. 22). The most significant aspect of these results is that the performance is predictable and that the exact effect on performance of the adjustable parameters is accurately known.

This method of circuit design is particularly well suited to power combiner design since it generates the impedance (or admittance) presented to the diode in a multidiode environment. An example of pertinent impedance data for the two-diode rectangular-cavity combiner is shown in Fig. 23. Impedance data is shown on a Smith chart. The chart contains half of the entire complex plane (the half for which real numbers are positive). When impedances are normalized to 15 Ω and plotted on a Smith chart, Fig. 23 is obtained. The diode package equivalent circuit is shown, along with measured diode impedance over a 2 GHz bandwidth. Actually, the negative of the diode impedance $(-Z_{diode} > 0)$ is shown for both a packaged and an unpackaged diode, as a function of the rf voltage across the diode for three discrete frequencies, 43.5, 44.5 and 45.5 GHz. The cavity impedance (impedance at points AA and BB in Fig. 15) for a two-diode combiner is shown for the same frequency range. If the cavity impedance is tranformed in such a way that the resulting
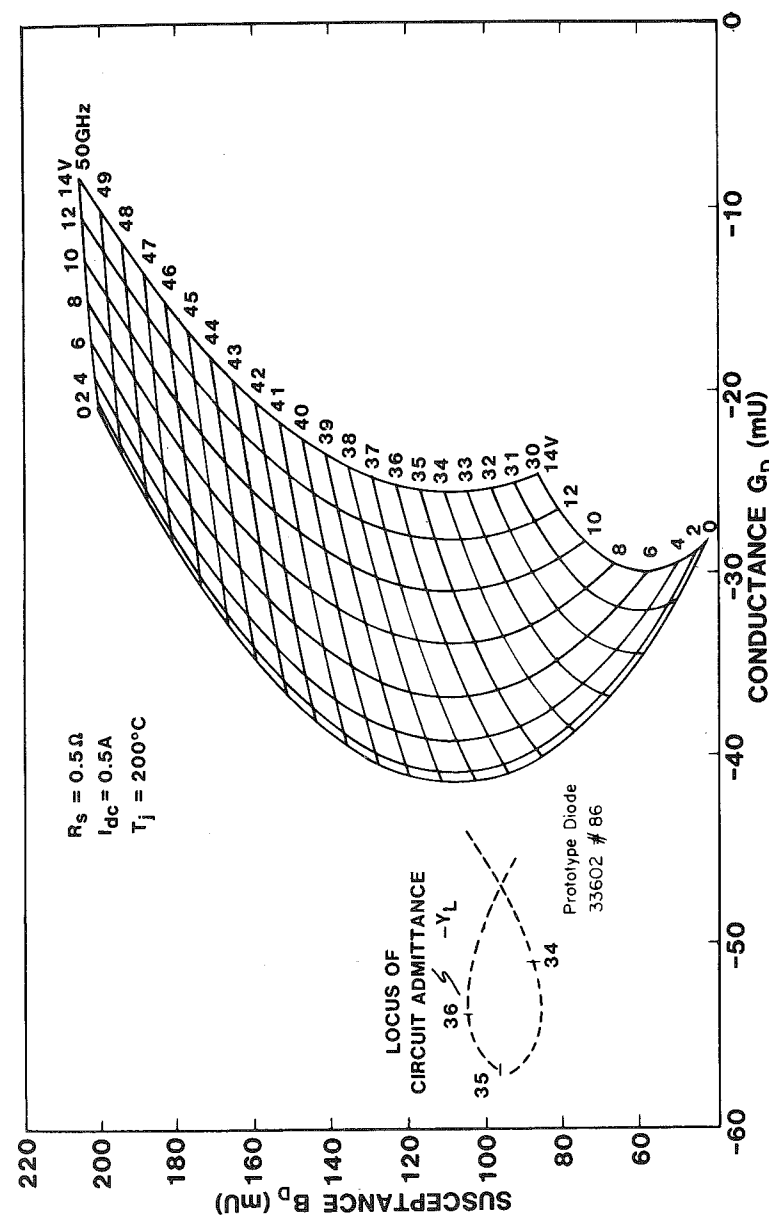

Figure 20. Admittance plane for a 35-GHz amplifier. (The device lines were generated by a computer model of the IMPATT diode.)
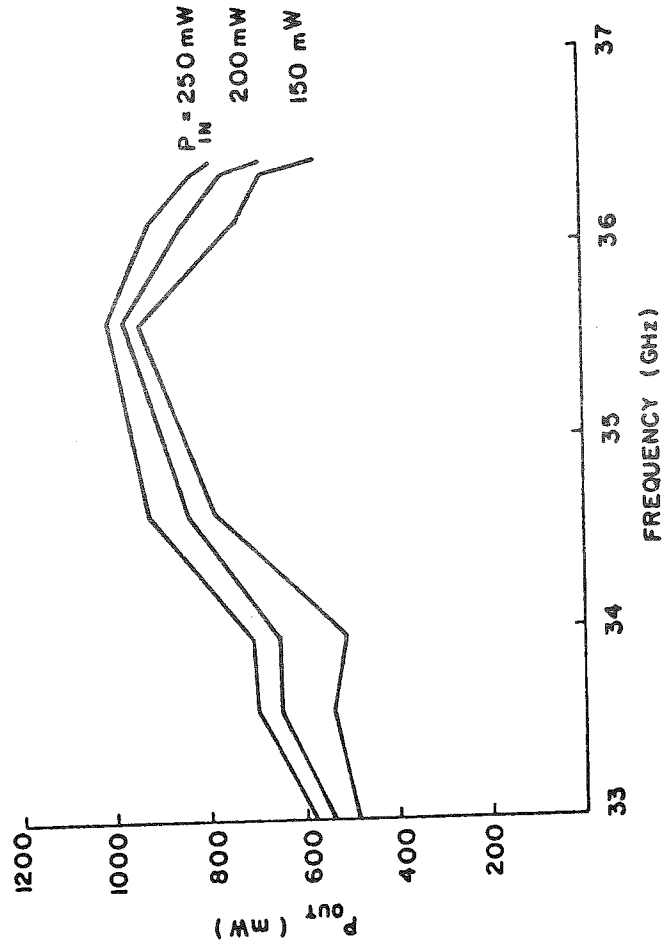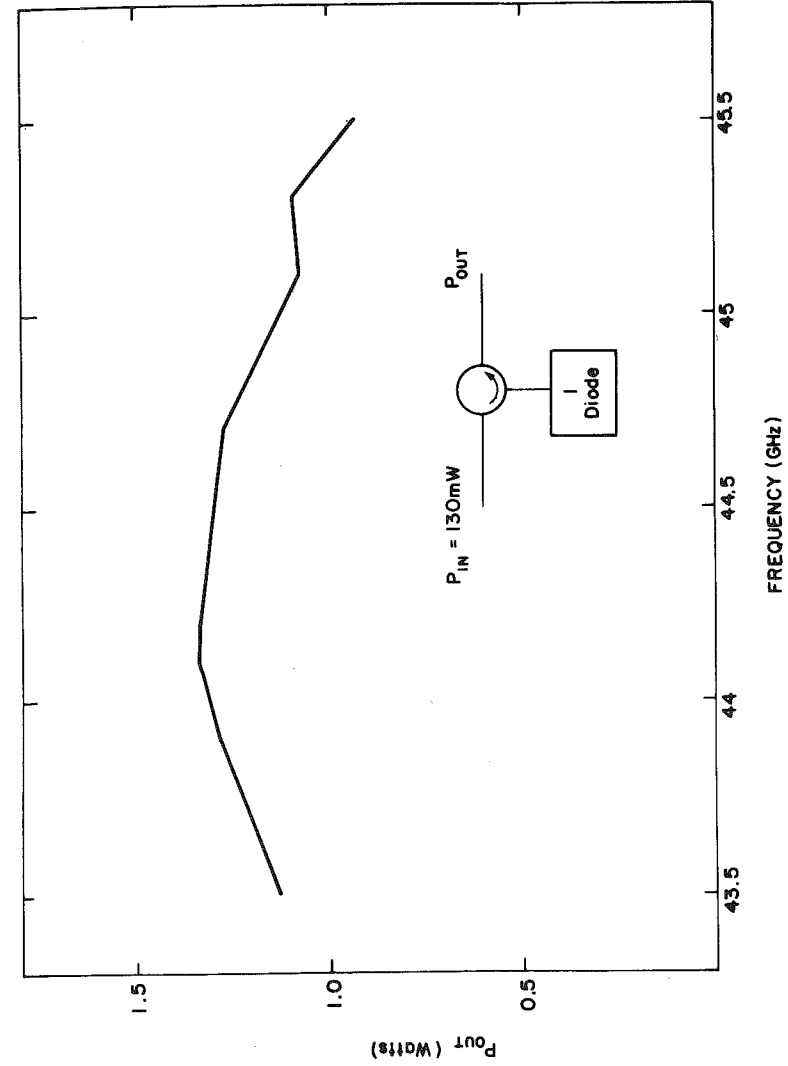
Figure 21.   35-GHz amplifier performance.

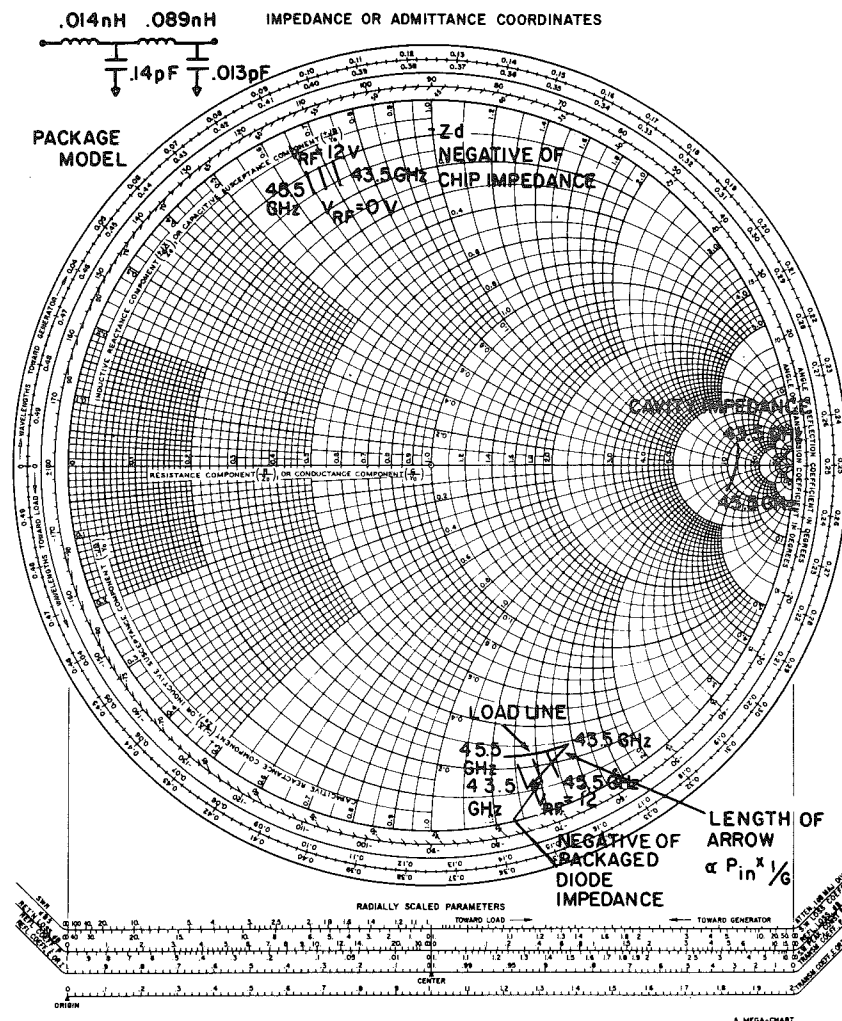Figure 22.   Single-diode (reduced waveguide height) circuit performance.

Figure 23. Circuit/diode matching for amplifier
operation (15Ω impedance chart).

impedance locus (the load line) intersects the negative of the diode impedance at some common frequency, the circuit operates as an oscillator at that frequency. The oscillator output power varies according to the exact position of the intersection. If the intersection occurs in the larger V_{rf} region (around 10-12 V), maximum power is obtained. As the intersection moves toward 0 V_{rf}, the oscillator power drops. In this case, an input signal may be provided to "connect" (in Fig. 23) the large V_{rf} points with the load line (at the same frequency, of course). This situation corresponds to amplifier operation. The further the load line is located from the diode's maximum power point, the larger the input signal must be to "bridge" this distance, and hence, the lower the amplifier gain will be (for maximum added power). For the diode-cavity match shown in Fig. 23, the relative position of the load line and the diode impedance was such that the circuit performed as a negative resistance amplifier. It produced ~3 W output power and 5 dB gain at band center. $Z_{circuit}$ at the reference plane of the packaged diode barely touched the diode impedance at 44.5 GHz and $V_{rf} \approx 0$, and hence, without an input signal, the added power was insignificant. The circuit was retuned for higher gain (~ 8 dB at band center); the performance obtained is shown in Fig. 24. Maximum power is still ~3 W; however, the mode of operation is conditionally stable the price we must pay for the higher gain. The narrow band response shown in Fig. 24 is indicative of the performance obtainable with cavities.

The accuracy with which a combiner can be characterized is demonstrated in Figs. 25a and 25b. These figures show efficiency and diode line impedance (at ports AA and BB Fig. 15b). A family of these curves is shown, indicating:

1. Repeatability of measurements during a single session.
2. Repeatability after cavity disassembly and reassembly.
3. Repeatability of measurements performed on different days after the equipment has been recalibrated.

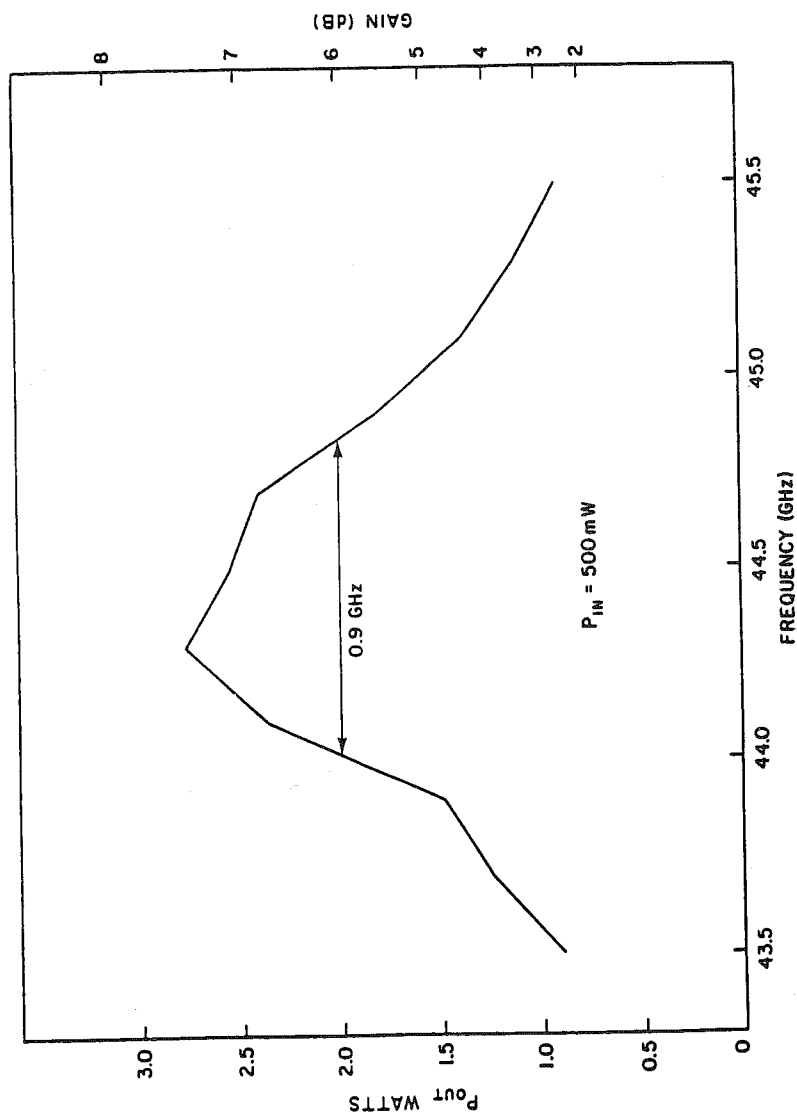Excellent agreement has been obtained. This agreement is remarkable considering the high frequency and the

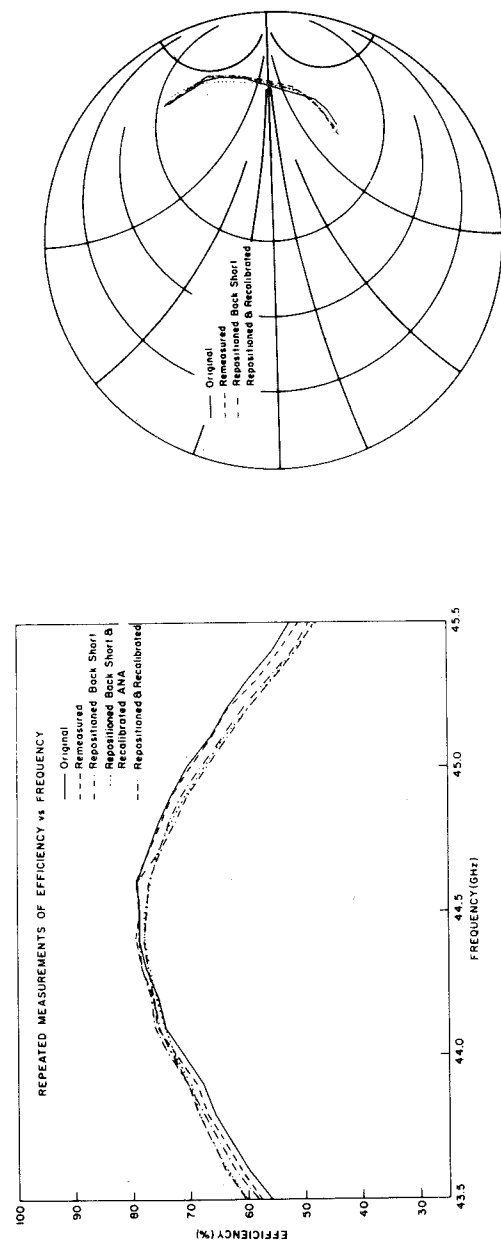Figure 24. Two diode combiner performance.

Figure 25b. Repeated measurements of midplane impedance (50 Ω chart).

Figure 25a. Repeated measurements of efficiency vs. frequency.

associated sensitivity to mechanical tolerances and assembly. Because these measurements are computer-controlled, they could be easily incorporated into a production-line check for cavity quality.

For a two-diode cavity resonating in the TE_{101} mode, the combiner efficiency and diode line impedance as a function of coupling iris size are shown in Figs. 26a and 26b. To realize the efficiency shown in Fig. 26a, the signals at each of the diode ports must be of equal amplitude and phase. In practice, some additional losses are introduced because of differences in diode characteristics and mechanical tolerances. Hence, Fig. 26a shows the highest efficiency achievable when the combiner is operated as an oscillator. Figure 26a shows that the maximum combiner efficiency increases as the coupling iris diameter is increased from 0.089 in. to 0.101 in. and then decreases with further increase in the iris size. For a small-diameter iris (0.089 in.), the loss in the cavity walls dominates. For a large iris (0.140 in.), it is the loss in the terminating loads which dominates.

It can also be seen from Fig. 26a and 26b that as the iris size increases, broader bandwidth can be achieved. First, the efficiency flattens over the band. Second, the variation of the cavity impedance with frequency is reduced for larger irises. This results in shorter load lines and flatter gains, but there is a practical limit to the maximum iris size that can be used because of the decrease in circuit efficiency. It is also difficult to obtain gains in excess of 5 dB with a very large -2liris because of the large impedance transformation required between the cavity and the diode. As the iris size increases, the cavity impedance "moves" toward the center of the Smith chart (Fig. 26b) and hence one needs a lower impedance transformer to match the diode. The minimum impedance transformers that can practically be made are 5-8 Ω. A solution to this problem is to "double-tune" the cavity. This can be accomplished with two coupling irises properly spaced as shown in Fig. 27. Pertinent impedance data in such a cavity is shown in Fig. 28, and performance is shown in Fig. 29. When one compares Figs. 23 and 28 with Figs. 24 and 29, one can easily see the broadbanding effect of the double iris configuration.

Using the design approaches previously described, a 2W amplifier was designed. To obtain a 2 W minimum from
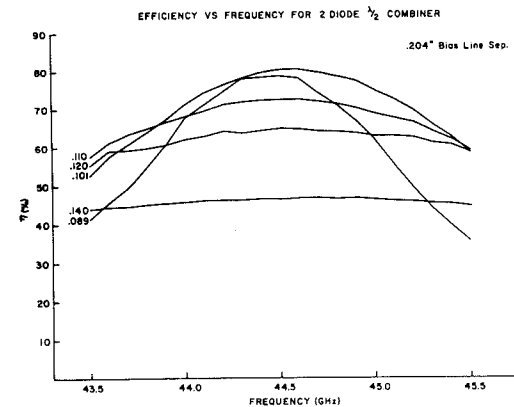
Figure 26a.   Efficiency vs. frequency for two-diode combiner.
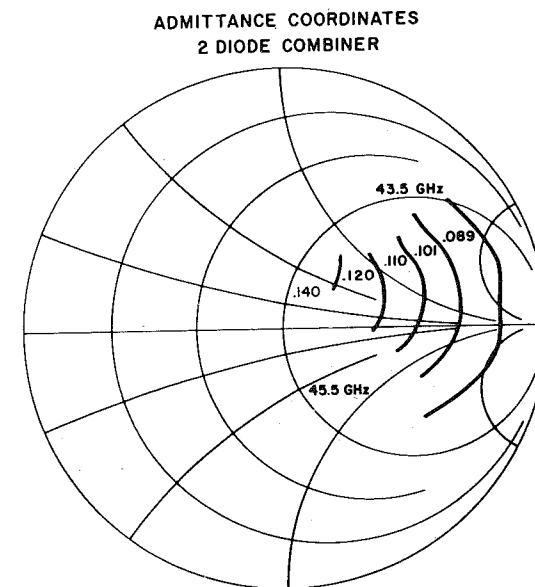

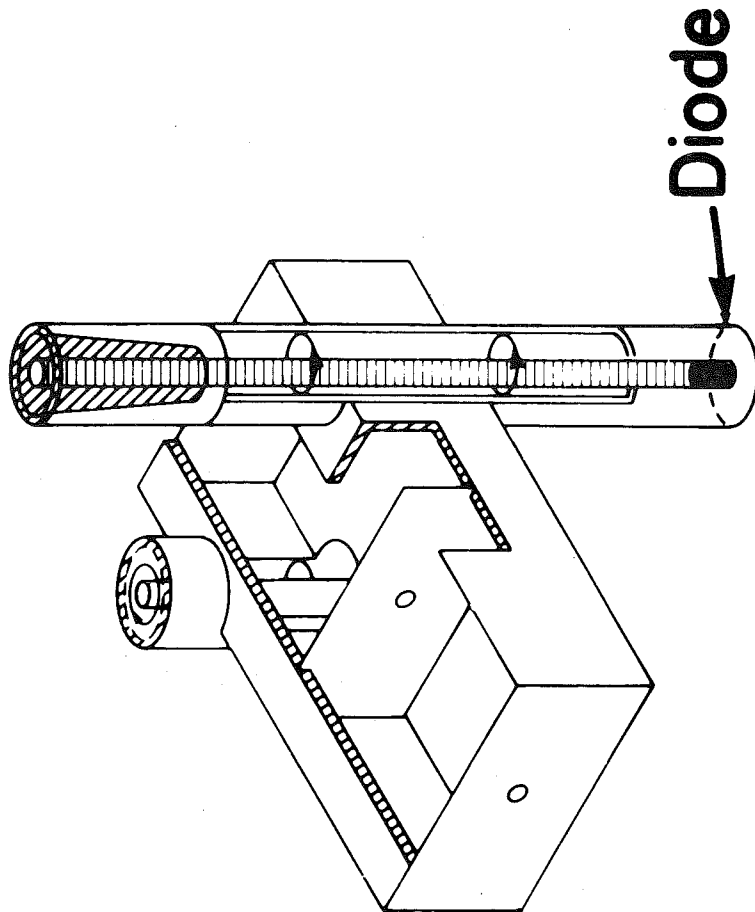Figure 26 b.   Midplane impedance vs. iris (50 Ω impedance chart).
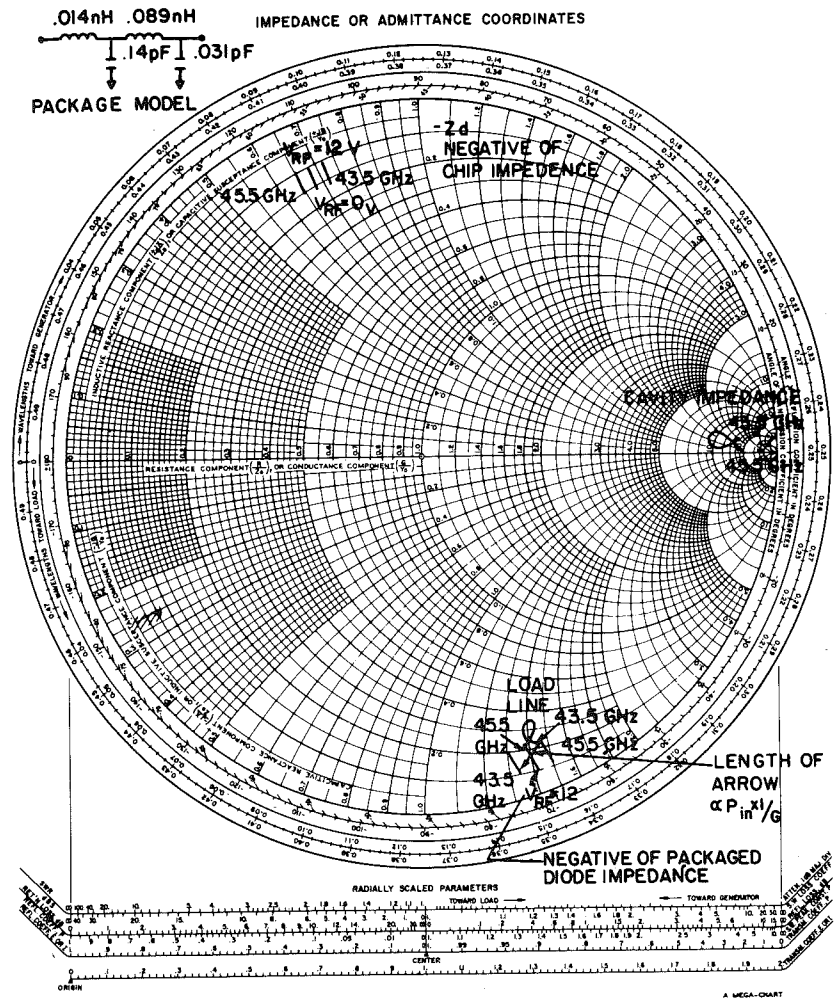
Figure 27. Double tuned 2 diode combiner circuit.

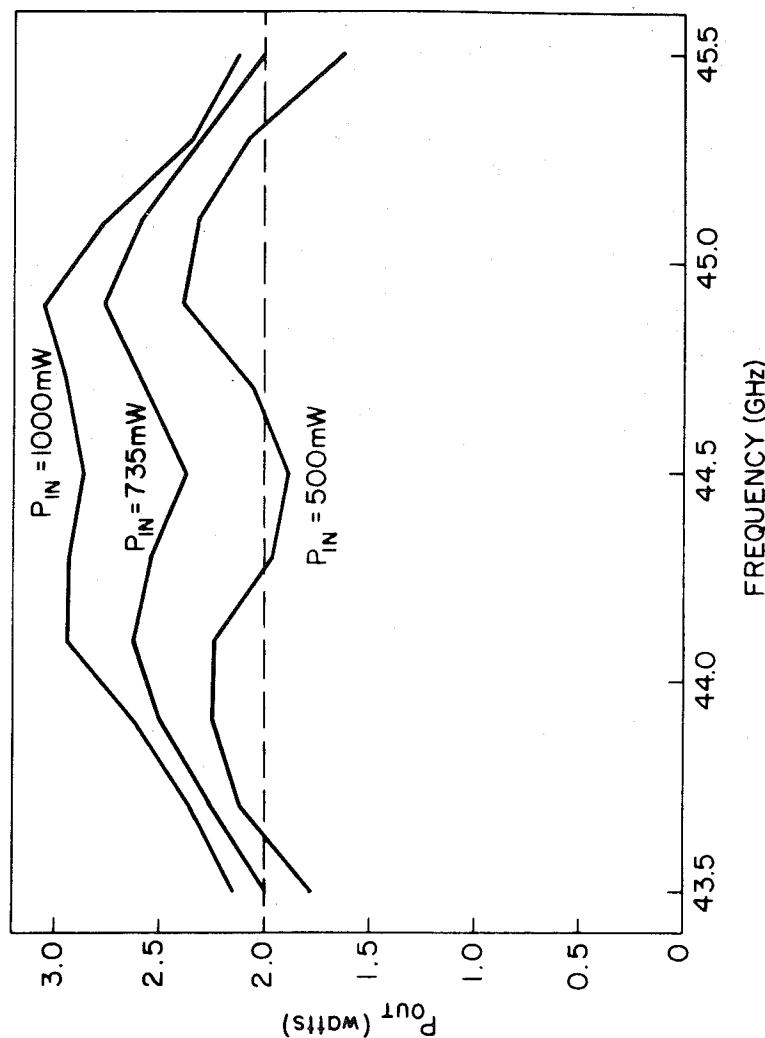Figure 28. Matching for a double tuned amplifier circuit.

43.5 GHz to 45.5 GHz, two IMPATT diodes in the output stage were needed. The combiner circuit was a rectangular wave-guide cavity type. A single diode in a reduced waveguide height circuit was used as the first stage. An isolator was placed between the two stages to prevent their inter-action. The amplifier block diagram and performance are shown in Fig. 30. Two watts minimum were obtained simul-taneously with a minimum gain of 12 dB. Maximum gain was 14 dB. This combination of power, bandwidth, gain and gain flatness makes this amplifier suitable for communi-cations applications. The fact that this performance was achieved with only three IMPATT diodes advanced the state of the art.

A product designed version of this amplifier is shown in Fig. 31. The compact, integrated three-junction circu-lator was developed by SMDO, Raytheon's Special Microwave Device Operation. This circulator is also a state-of-the-art design.

To achieve higher power levels (~ 25–50 W), the out-put powers of several single- and two-diode circuits can be combined. It is also possible to combine larger numbers of diodes in a rectangular cavity and then combine the powers of these higher power "building blocks". The best approach to follow will depend on specific requirements.

Conclusion

Because of its higher efficiency, the GaAs IMPATT diode is a suitable choice for power generation when re-liable operation is required. The characteristics of these diodes were discussed along with their various modes of signal amplification. Power added by the diodes, gain, bandwidth, and stability were shown to be interrelated, and to be controllable by the circuit in which the diodes are embedded.

Two single- and two multi-diode circuits were dis-cussed. A single-diode circuit, the so-called "tophat", is a good choice for a diode test circuit. A second single-diode circuit, which uses reduced-height-waveguide struc-tures, is capable of broad bandwidth and is, therefore, well suited for the first stage in an IMPATT amplifier chain. The multidiode circuits discussed were both rec-tangular and cylindrical cavity combiners, suitable for high power amplifier stages.

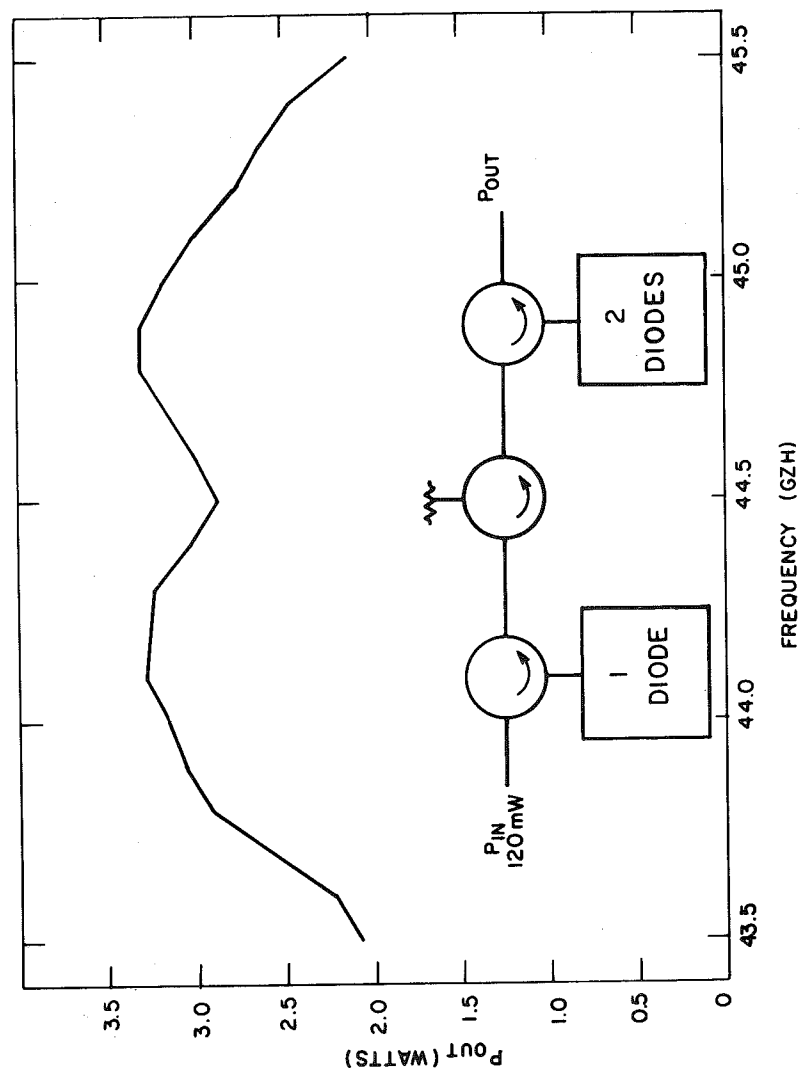Figure 29. Two-diode combiner performance.

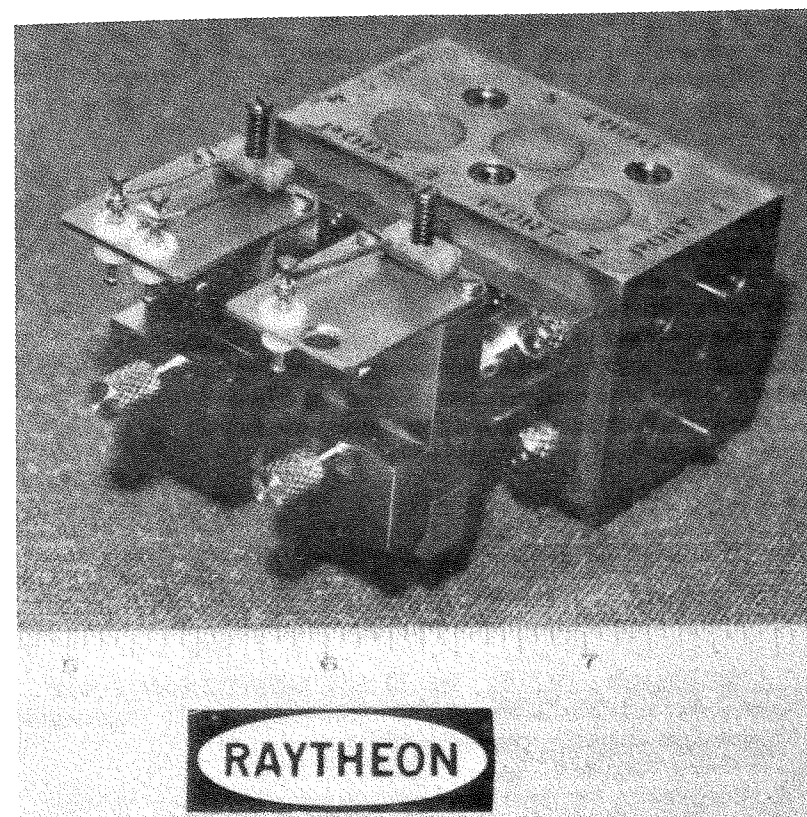Figure 30.   2 W, amplifier performance and block diagram.

Figure 31.   2 W, 2 stage Q-band IMPATT amplifier.

It was shown that it is possible to design these circuits for predictable performance. Examples of state-of-the-art performance achieved by Raytheon were also given.

References

1.   C.A. Drubin, A.L. Hieber, G. Jerinic, and A.S. Marinilli, "1 kW Peak 300-W Average IMPATT Diode Injection Locked Oscillator", 1982 IEEE MTT-S International Microwave Symposium Digest, pp. 126-128.

2.   "Ku-Band Amplifier Development", Technical Report AFAL-TR791173, Final Report for Period May 1978 - April 1979, Air Force Avionics Laboratory, Air Force Wright Aeronautical Laboratories, Air Force Systems Command, Wright-Patterson Air Force Base, Ohio 45433.

3.   G. Jerinic, J. Fines, M. Schindler, "3 W, Q-Band Solid State Amplifier", 1983 IEEE MTT-S International Microwave Symposium Digest, pp. 481-483.

4.   J. McClymonds, "A 16.5 W, 20 GHz IMPATT Diode Power Combiner", 1983 IEEE MTT-S International Microwave Symposium Digest, pp. 484-486.

5.   K. Kurokawa, "Injection Locking of Microwave Solid-State Oscillators", IEEE Proc. 61, (10), pp. 1386-1410.

6.   K. Kurokawa, "Power Waves and the Scattering Matrix", IEEE Transactions MTT-13, pp. 194-202, 1965.

7.   Kai Chang and Roy Ebert, "W-Band Power Combiner Design", IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-28, No. 4, April 1980.

8.   R. Adler, "A Study of Locking Phenomena in Oscillators", Proc. IRE 34, pp. 351-357 (June 1946).